Jitter and Latency Evaluation of Phasors Computation in Power Systems

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Abstract— This paper evaluates Jitter and Latency in a novel technique for computation of Phasors in power systems. The evaluation is done for dynamically computed Phasors based on streamed Sampled Measured Values provide by the Merging Units (MUs) installed in contemporary power substations. In this evaluation, the effects of Jitter and Latency introduced by the communication network on computed Phasor are tested by using two methods of measuring Jitter which are chosen to handle problems of clock offset and drift. Representative results in evaluating of Phasors computation performance are presented in this paper.

I. INTRODUCTION

THE computation of Phasors by the conventional static methods [1][2][3] is not efficient where these conventional methods were not designed to capture the dynamic changes in power system state variables (i.e. bus voltage magnitude and phase angle). Nowadays, the dynamic changes in Phasors can be monitored directly by means dedicated instruments such as Phasor Measurement Units (PMUs). Today, using the stand-alone PMUs for a robust monitoring the dynamic change in Phasors can be replaced by of Phasors computation using the IEC61850-9-2 Sampled Measured Values [4] streamed from the various MUs at Process-Bus (Figure 1). This computation can is done at a central substation process computer for all measurement points (i.e. MUs) in a power substation. The measurements deliver to the central substation process computer from the bay-level by using what is called Process-Bus that is Ethernet-based technology. The MUs are converting the analogue voltage and current waveforms into the sampled

measured values and then multicast them on the substation Local Area Network (i.e. Process-Bus).

The delivery of the streamed values may be done by using copper wiring or by using serial communication. Two kinds of transmission are supported for transfer streamed values: a Multi-cast service (MSVC) over Ethernet and a Unicast (point-to-point) service (USVC) over serial links. According to the IEC 61850-9-2 implementation guide [5], the streamed values are standardized at sample rates 80 Samples/Cycle and 256 Samples/Cycle. Delivery of stream values can be accomplished by using Distributed Reservation Protocol (DRP), where nodes have access to the medium in re-served slots, or Prioritized contention access (PCA), that provides differentiated, distributed contention access to the medium. While clocks are used to trigger sending sampled values in a power system, the Phasors relationship (phase relationship) between the different computed Phasors of the signals (in particular between current and voltage) is very important aspect which should be taken into the account.

This relationships are highly affected by the clocks offset and drift accuracy which should be corrected. IEC 61850 is using the concept of synchronisation. All nodes perform sampling should be synchronised to global clock with the required accuracy to guarantee that the samples are taken all at the same time. One of the typical applications of the Process-Bus communication is transferring the between instrument transformers and protection devices. This information transferred is a time critical and its impacts on the response time and accuracy of the protection function is significant due to the Jitter and Latency in the delivered information. Evaluating the impacts of Jitter and Latency is

very important to guarantee a robust operation to the protection system.

In this paper, an evaluation of the impacts of the Jitter and Latency in an alternative approach for Phasors computation is done based on the IEC61850-9-2 Sampled Measured Values which has been used to provide a dynamic state estimation in power utilities today.

The paper is structured as follows: Section II present some overviews of the IEC61850 Process-Bus. Section II also gives an overview of Kalman Filtering and how it can be used and fitted. Section III is preliminary tests and performance evaluation. In this section, the impacts of Latency and Jitter errors on the performance of the computed Phasors have been evaluated and some other important aspects like time response performance and steady-state error accuracy also verified. Section VI is the conclusions.

II. OVERVIEW OF IEC 61850 PROCESS BUS AND UNSENTED KALMAN FILTERING MODEL-BASED DESIGN

A. Overview of IEC 61850 Process Bus

IEC 61850 [6] is the world-wide accepted standard for the communication within the SAS. In general, the IEC 61850 standard consists of two kinds of communication, Process-Bus and the Station-Bus which both are Ethernet technology supported. The conceptual architecture of the Process-Bus and the Station-Bus is shown in Figure 1. The Process-Bus applications of the IEC 61850 require synchronized sampling processes for the current and voltage acquired from the high voltage equipment (electronic instrument transformers and the MUs). The MUs are converting the analogue voltage and current waveforms, position and open/close controls into the sampled measured values and then multicast them on the substation Local Area Network (*LAN*).

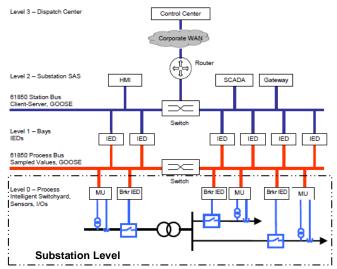


Figure 1 Process Bus and Station Bus in the IEC 61850-based SAS

B. Overview of Kalman Filtering

Kalman Filtering (KF) [7-9] is a mathematical technique widely used to compute the optimal estimates of a dynamic system states. The estimates are optimal in the sense that estimation errors are minimized in the least-squared sense. The dynamic system can be described and show how its states change with time by using a set of linear differential equations (in vector and matrix format) as follows:

$$\dot{\mathbf{x}} = \mathbf{F}\mathbf{x} + \mathbf{w} \tag{1}$$

where

 \boldsymbol{x} is the state vector.

F is the system matrix.

w is a random driving noise vector.

Equation (1) is also known as the "Process Model".

Suppose that our power system have various kinds of sensing nodes to measure specific quantities (voltage and current waveforms). These measurable quantities can be related to system states by the following set of linear equations.

$$z = Hx + v \tag{2}$$

where.

z is the measurement vector. Each variable in this vector represents quantities measurable by sensing nodes.

H is the measurement matrix.

v is a random vector describing measurement noises.

Equation (2) is known as the "measurement model". At present, equations (1) and (2) are expressed in continuous-time. To calculate system states at a particular point in time, equations (1) and (2) need to transformed to discrete-time model. It can be shown that the discrete time model of (1) and (2) can be expressed as.

$$\begin{aligned}
\mathbf{x}_{k+1} &= \emptyset_k \, \mathbf{x}_k + \mathbf{w}_k \\
\mathbf{z}_k &= \mathbf{H}_k \, \mathbf{x}_k + \mathbf{v}_k
\end{aligned} \tag{3}$$

where

 x_k is the system state vector at time t_k .

 \emptyset_{k} is the state transition matrix and it can be computed from $\emptyset_{k} = e^{F.\Delta T} \approx I + F \Delta T$, where $\Delta T = t_{k+1} - t_{k}$ is the time-step (In our simulation, it will be 0.02/80 or 0.02/256)

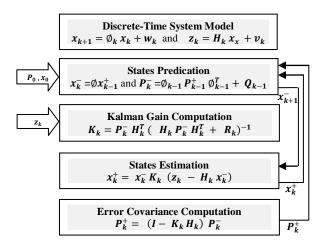
 \mathbf{z}_k is our measurements vector at time t_k .

 $\boldsymbol{H_k}$ is the measurement matrix at time t_k .

If the driving noise w_k and measurement noise v_k are defined in stochastic terms, then, KF algorithm requires w_k and v_k to be random processes with the following characteristics:

- Zero-mean
- Gaussian (Normal) distribution
- White (Uncorrelated)
- w_k and v_k have covariance matrix of are Q_k and R_k , respectively.

The Kalman Filtering algorithm process is given by:



 x_0 and P_0 must be determined before starting KF.

One basic and important requirement of standard KF algorithm is that both the process and the measurement models are linear as shown in (1) and (2). However, signals in our system are nonlinear (Voltage and Current Sinusoidal Signals). In such cases, adaptation to the standard algorithm is required, so it can to be used within our system. A more recent development known as Unscented Kalman Filtering (UKF) [7, 8] can overcome the weakness of traditional Kalman Filtering (Performance deteriorates drastically under highly nonlinear system).

Instead of using linearized equations to approximate the nonlinear model as traditional Extended Kalman Filtering (EKF) approach, UKF generates a finite set of points called as sigma points. These sigma points are transformed to a new set of points using the nonlinear model. System states and associated error covariance matrices are determined numerically based on the mean and covariance values of the transformed sigma points. Mathematically, the UKF process can be presented as follows.

The predicted states x^- is computed by defining 2n sigma points $x_{k-1}^{(i)}$ from $x_{k-1}^{(i)} = x_{k-1}^+ + x^{-(i)}$, i = 1, ..., 2n

where

$$\mathbf{x}^{\sim(i)} = \left(\sqrt{n \, P_{k-1}^{+}}\right)_{i}^{T}, \ i = 1, \dots, n$$
 (5)

$$\chi^{\sim (n+i)} = -\left(\sqrt{n} \, P_{k-1}^+\right)_i^T, \ i = 1, \dots, n$$

These sigma points and the nonlinear process equation are used to transform to 2n sigma points $asx_k^{(i)} = f(x_{k-1}^{(i)}, t_k)$, then the predicted state vector is computed from

$$x_k^- = \frac{1}{2n} \sum_{1}^{2n} x_k^{(i)}$$

C. UKF Model-Based Design for DSE

The proposed model for Phasors estimation is based on Unsented Kalman Filtering and can be used for estimation of single or three phase power systems. The significance of this Kalman Filtering model is that all state variables (Magnitude, Phase and Angular Frequency) of signals provided by all different measuring nodes can be estimated at once. This Filtering does not have the stability problems like the nonlinear one of Kalman Filtering. The algorithm is tested through different computer simulations including with the data collected from the substation model. The three-phase signal voltage or current of power system can be represented as:

$$v_a(k) = v_m \sin(wk\Delta t + \emptyset) + \in_a (k)$$
 (7)

$$v_b(k) = v_m \sin\left(wk\Delta t + \emptyset - \frac{2\pi}{3}\right) + \epsilon_b(k)$$
 (8)

$$v_c(k) = v_m \sin\left(wk\Delta t + \emptyset + \frac{2\pi}{3}\right) + \epsilon_c(k)$$
 (9)

where $\in_a (t) \in_b (t)$ and $\in_c (t)$ noises that can be white noise, Δt is the sampling time (0.02/80 or 0.02/256).

The $\alpha - \beta$ components are obtained for these discrete as

$$\begin{bmatrix} v_{\alpha}(k) \\ v_{\beta}(k) \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{\alpha}(k) \\ v_{b}(k) \\ v_{c}(k) \end{bmatrix}$$

The discrete complex voltage signal v(k)

$$v(k) = v_{\alpha}(k) + jv_{\beta}(k) \tag{10}$$

$$v(k) = A e^{j(wk\Delta t + \emptyset)} + \eta(k)$$
(11)

$$Ae^{j(wk\Delta t + \emptyset)} = A\cos(wk\Delta t + \emptyset) + jA\sin(wk\Delta t + \emptyset)$$

Let $y = A\sin(wt + \emptyset)$ and assume that $x_1 = wt$, $x_2 = w$, $x_3 = A$ and $x_4 = \emptyset$. If these Magnitude, Phase and Angular Frequency of the sinusoid signal are assumed to be constants, than, it can be write

$$\dot{x}_1 = w$$
, $\dot{x}_2 = 0$, $\dot{x}_3 = 0$ and $\dot{x}_4 = 0$

The discrete-time processes model is

The discrete-time measurement model is

$$\mathbf{z}_{k} = [x_{3}\sin(x_{1} + x_{4})]_{k} + [v_{x}]$$
 (12)

The generalized model for n nodes can be written as:

III. PRELIMINARY TESTS AND PERFORMANCE EVALUATION

In this section, many Jitter and Latency have been tested and evaluated to show their effects on the performance. Testing the performance has been done with respect to Latency. To evaluate the performance, several kinds of simulation were realized to test the effect of number of nodes, on the communication network and hence Phasors computation. These tests will show how the simulator is in compliance with IEC61850 and guarantee that benefits of IEC61850-9-2 and UKF to produce dynamic monitoring at substation control center with minimum cost are satisfied.

1) - Latency and Jitter Test:

Jitter is the variation in the Latency of packets at the receiving nodes. If the Jitter value is high, the performance in some time-sensitive power applications might get affected. IEC61850-9-2 implementation guide has specified Jitter value to be < 20ns and maximum Latency of 3 millisecond. So, this test will show how this configured system is in compliance with IEC618509-2 implementation guide. To

accomplish the test, bout 250 packets had been used and each packet with six SMV. Also, the Latency introduced by the network is checked at the chosen maximum number of nodes (Sixteen Nodes). It's clear from Figure. 2 that the maximum Latency is below the threshold value which is specified by IEC61850 (3 millisecond). For this selected number of packets, there are only five packets with high value of maximum Latency above the half value of the threshold. In our application, the Phasors are updated with every arriving SMV which is in the ideal case 0.25 millisecond.

According to C37.118 standard, Phasors must be updated and provided 60 times per second (or every 16 millisecond). Depending on the case that the updating occurs at the time of receiving the SMV and if there is five SMV with a Latency of about 2 millisecond as the case in Figure 2, this can leads to decreasing the updating frequency to 59 times per second. The worst case is happened when a Latency of 3 millisecond is introduced in the network.

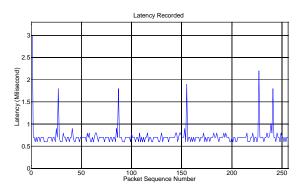


Figure 2 Latency introduced by the network at sixteen nodes and six SMV per frame

Two methods of measuring Jitter had been chosen based on parameters being taken into and in each way. *Method#1* is the difference in maximum and minimum Latency. In this method, Maximum Jitter is the difference in the maximum and minimum Latency measured over a testing interval. The most common calculation is as follows.

$$Jitter = Maximum Latency - Minimum Latency$$
 (13)

Here, Latency is calculated over the whole test duration. Simulation results of applying this method on the proposed system under IEC61850-9-2 communication. *Method#2* calculates Jitter as the change in the deference in the arrival time of the packets (Equation 14). This method of measuring Jitter takes into account, the arrival time and not the Latency.

$$Jitter_n = |\Delta arrival_n - \Delta arrival_{n-1}|$$
 (14)

where, $\Delta arrival_n = |arrival_n - arrival_{n-1}|$

Result of both methods is shown in Figures 3 &4. It's clear that both graphs have an occurrence of Jitter value close to ten nanosecond and the occurrence is greater in *method#2*

than *method#1*. In both methods, the maximum Jitter is less than 20 nanosecond in both methods.

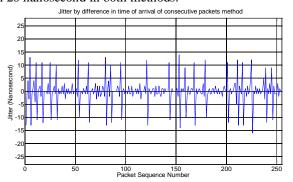


Figure 3 Jitter recorded by using method#1

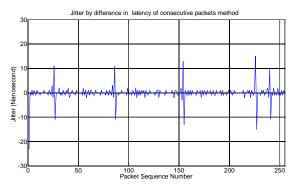


Figure 4 Jitter recorded by using method#2

Method#1 obtains the difference found between the maximum and minimum Latency. This method is the easiest way of measuring Jitter and produces reasonably acceptable values. Method#1 gives dependable measurements. Method#2 only takes the current and previous two arrival times for the measurement and not the Latency. Hence the effect of spike (Method#1) does not propagate through the entire distribution. However, this method gives too large values for saw tooth type of measurements and does not reveal the actual behaviour. The results are summarized in histograms shown in Figures 5&6.

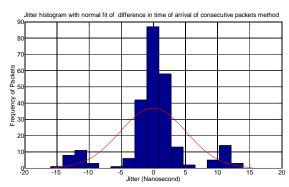


Figure 5. Jitter histogram of mothod#1

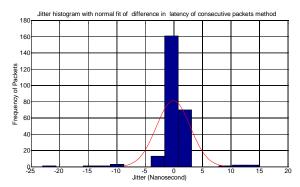


Figure 6. Jitter histogram of method#2

IV. CONCLUSIONS

Evaluating and testing the impacts of Jitter and Latency on a Novel technique for Phasors computation based on streamed Sampled Measured Values in contemporary power substations has been presented in this paper. The impacts of Jitter due to substation clock error on the computation of Phasors by using the sampled measured values that is delivered by the substation Process-Bus and to be used in the computation in the centralized computation has been examined. Also, the Latency introduced by communication of the Process-Bus itself and how it be compliance to the IEC 61850-9-2 implementation guide is tested. Both results showed that the errors are within the limits defined in the guide. These results can be used to tolerate the technique for Phasors computation as a new application and to add new function to the existing Substation Automation System.

V. REFERENCES

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